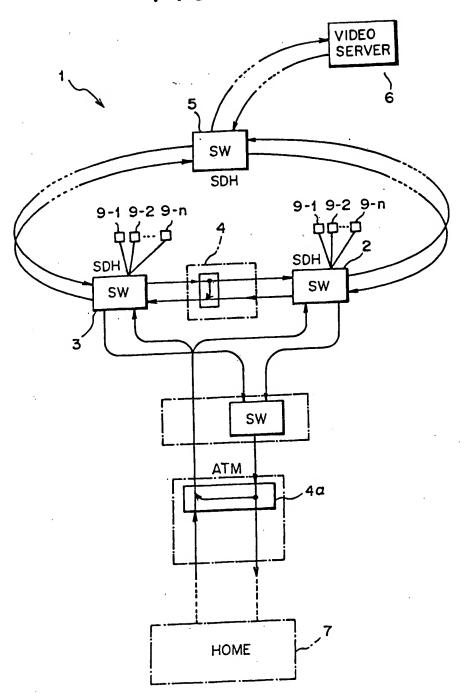
FIG. 1



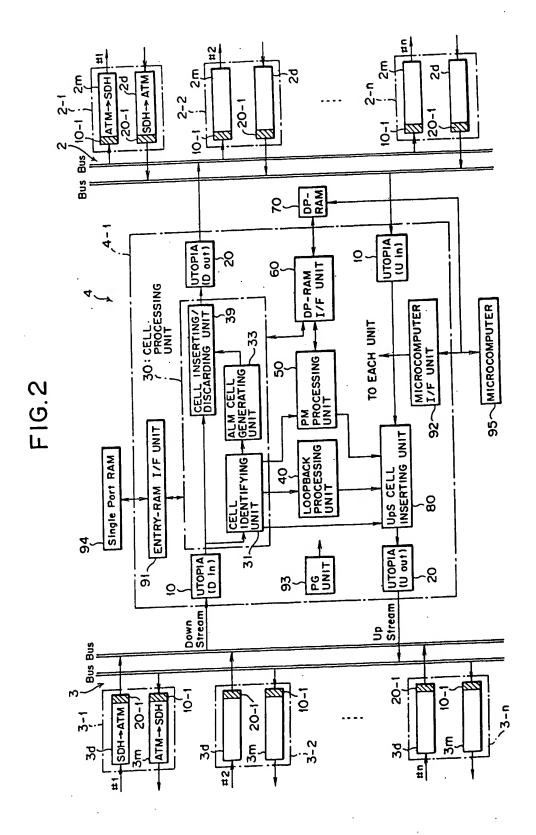


FIG. 3(a)

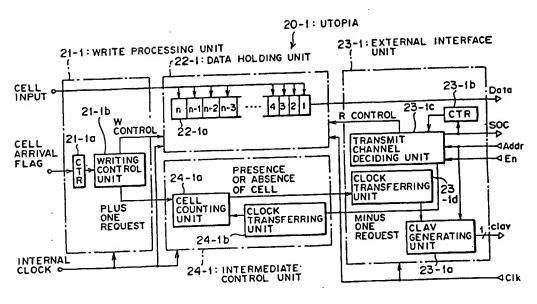


FIG. 3(b)

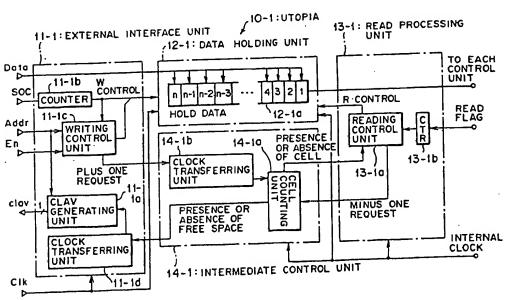


FIG. 4(a)

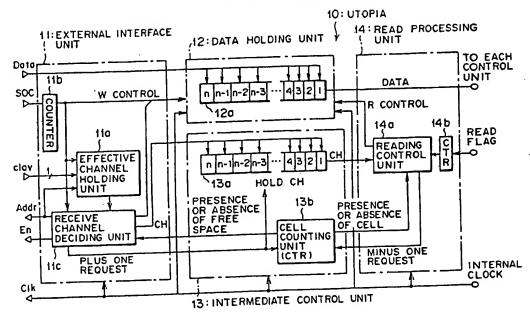
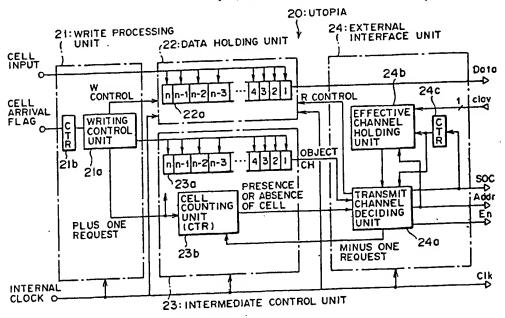
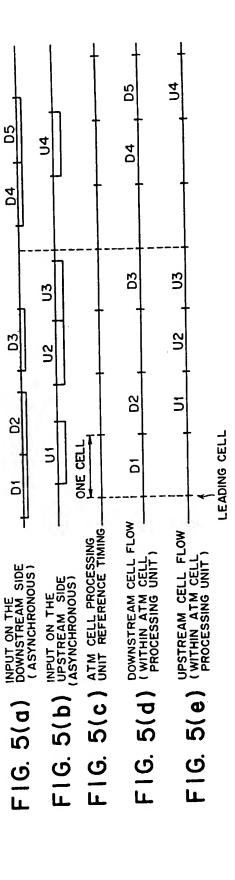


FIG. 4(b)





F16.6

FIG.7

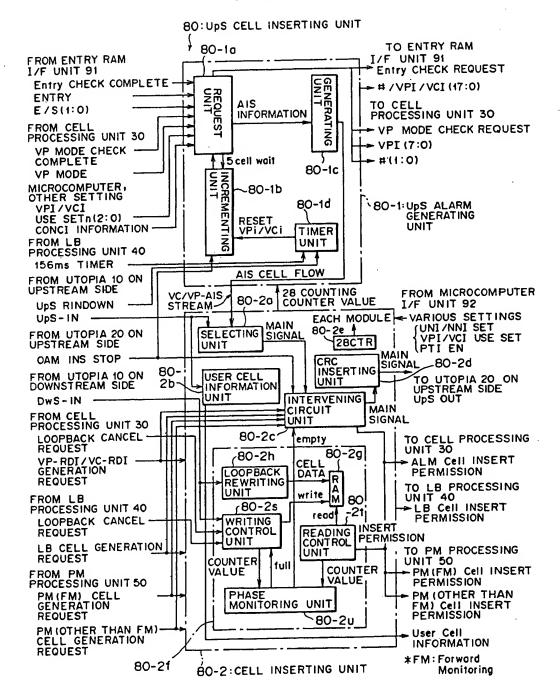


FIG.8

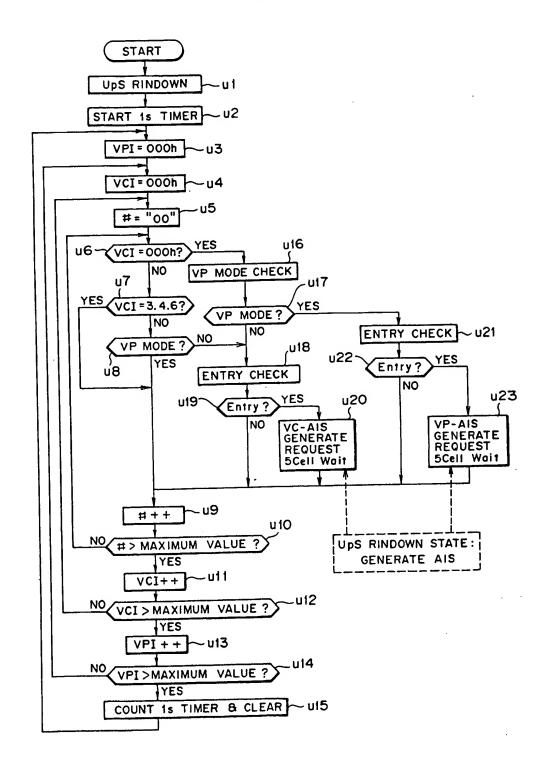
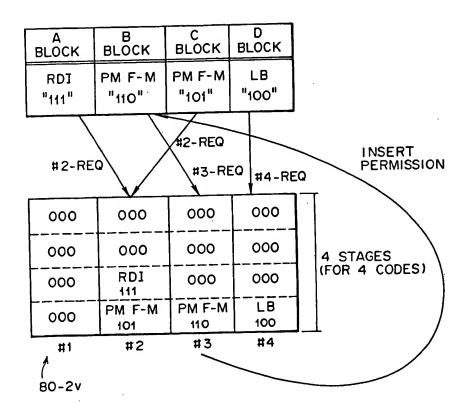


FIG.9



111 A BLOCK: CELL PROCESSING UNIT

110 B BLOCK: PM PROCESSING UNIT (FM)

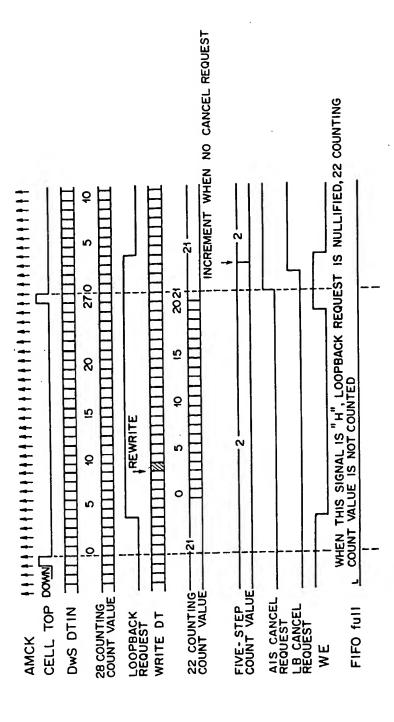
101 C BLOCK: PM PROCESSING UNIT (OTHER THAN FM)

100 D BLOCK: LB PROCESSING UNIT

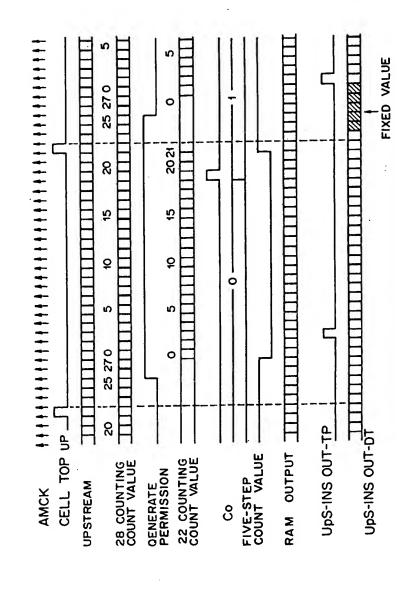
					(bit)			
(clk)	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	_ <del></del>	11 10 9 8	<del> </del>	
` á	GFC	VP	l 	VCI	GFC	VI		VCI
2		VCI		PTI CLP		VCI		PTI CLP
3	UDF1 (		UDF	2	1	(HEC)	UD	
4	OAM CELL	FUNCTION TYPE	DEFECT	TYPE	OAM CELL TYPE	FUNCTION TYPE	LOOPBAC	
5		•				RELATION	N TAG	
6						( 4 byte )		, , , , , , , , , , , , , , , , , , ,
7								
8	DE	FECT LO	CATION					
9		16 byte )	-					
10					LOOPB	ACK LOCA	TION ID (	OPTIONAL)
11						(16 by1	e / 	
12								
13								
14								
15								
16							<b></b>	
17		• • • • • • • • •						
18		UNUSE				CE ID ( OF	PTIONAL	)
19		( 20 byte	)			16 byte )		
20		"6A"						
21								
22								
23								
24		UNUSE				UNUS		
25		(8 byte	)			(8 by	ie ) 	
26		"6A"				<b>"</b> 6A		
27	RESERVED	000000"	RE-ATTAC	C - 10 )(00)	RESERVE	D <sup>*</sup> 0000000"	RE-ATTAC	CH EDC 01 ('OO')
28		DUMMY B	11 11			DUMMY BI		

23~ 28:RDI & LB CELL FORMAT COMMON FIXED PATTERN

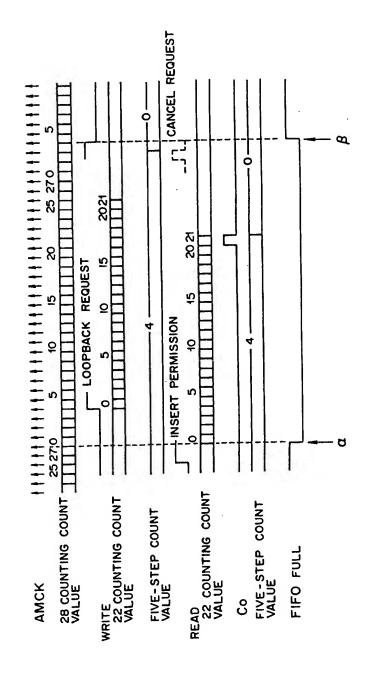
— Э



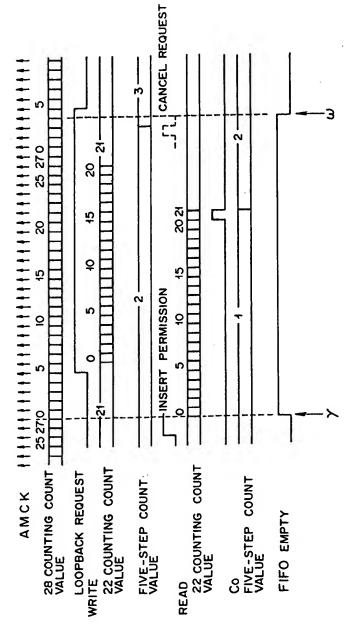
F16. 13

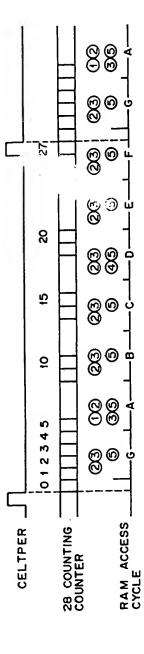


F1G. 14



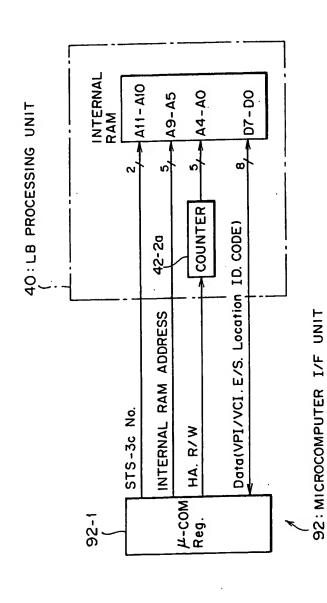
F1G. 15





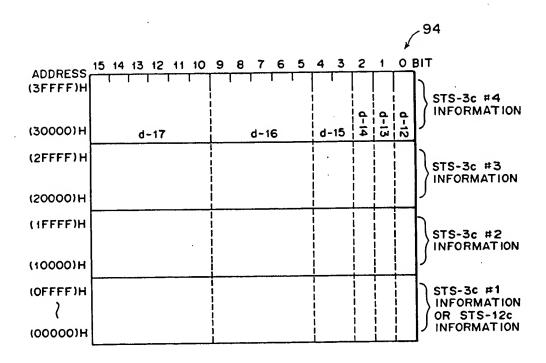
F16, 16

F16,17



F1G. 18

REG. STATE	READ/WRITE	READ/WRITE	READ/WRITE		READ/WRITE								READ/WRITE									READ ONLY
BIT 04, 03, 02, 01, 00	A ADDRESS		88	80		B120	8112	() B	968 		B80	B72	B64	B56	B48	B40	832	B24	B16	88	8	CODE
BIT 04,03,0	ڪا		- VPI/VCI -		E/S								LOCATION ID	( 16 byte )								
. 06 , 05	1"				พ่				8					2					9	2		
10	8	¥	815	87		B127	B119	= 0	B 103	895	887	B79	B71	863	B55	B47	839	831	823	815	87	
L S I ADDRESS	124	13H	14H	15H	19н	17H	18н	19н	1 A H	18H	1CH	104	EH	1FH	20H	21H	22H	23H	24H	25H	26H	27H



d-12: ENTRY: WHETHER VPI/VCI IS ENTERED ("H": IN PROCESS OF ENTRY)

d-f3: VC TERMINATION: WHETHER VPI/VCI IS TERMINATED. WHEN "H", VPI/VCI IS IN (End-to-End) SETTING.

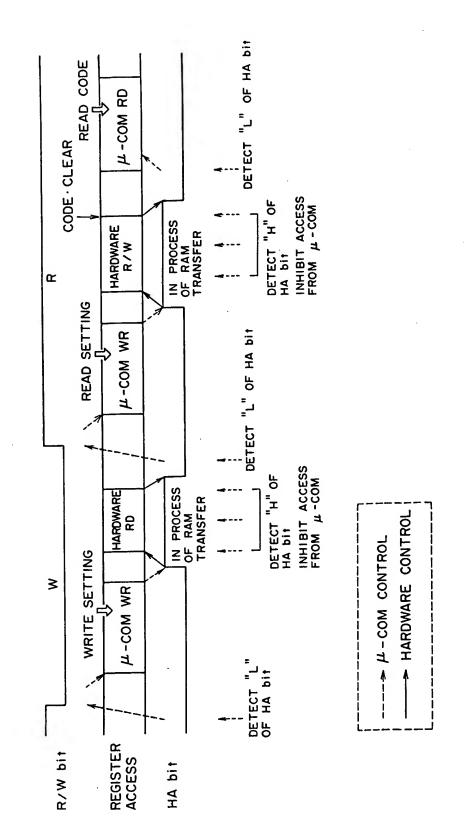
d-14: OAM INVALID:
WHEN "H", OAM CELL UNDERGOES NO PROCESS, PASSES THROUGH
WHEN DETECTED.

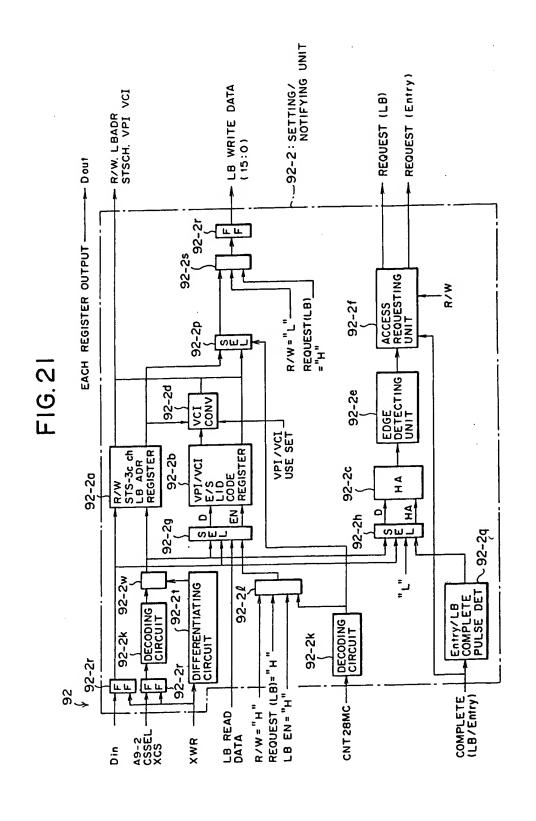
d-15: E-to-E/Segment:
 DESIGNATE End-to-End/Segment OF VPI/VCI. 2bits EXPRESSES
 4 STATES. ONLY TWO STATES OF "01" AND "11" ARE DETERMINED.
 THE OTHER STATES ARE HANDLED AS INVALID (NO Segment
 DESIGNATION)

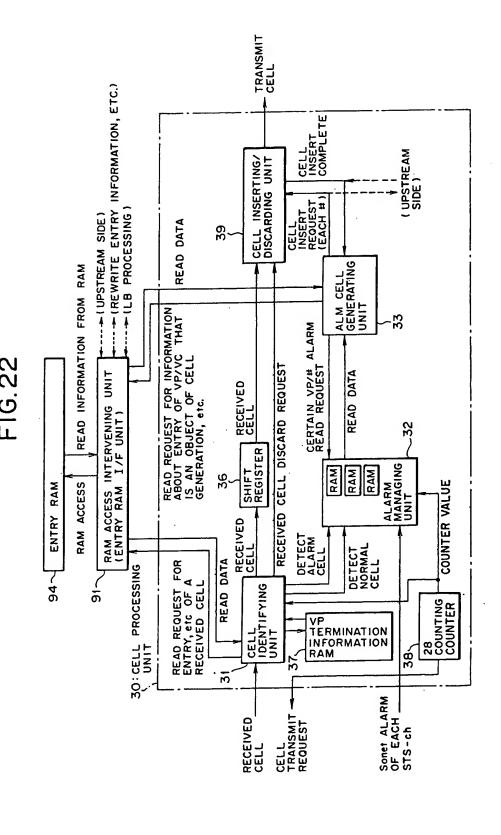
d-16: Loop Bock ADDRESS:
SHOW WHICH ch AMONG 32ch THAT ARE OBJECTS OF Loop Bock
VPI/VCI CORRESPONDS TO

d-17: VC ALM ADDRESS: SHOW WHICH CHANNEL AMONG 64ch THAT ARE OBJECTS OF VC-AIS/RDI DETECTION VPI/VCI CORRESPONDS TO

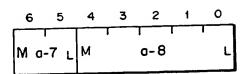
F16.20







## FIG. 23



a- 7: SHOW STS - 3c #

00: STS-3c #1 or STS-12C

01: STS-3c#2 10: STS-3c#3 11: STS-3c#4

q-8: VPI ( HIGH ORDER 5 bits AMONG 8 bits )

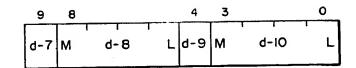
## FIG. 24

7	6	5	4	3	2	1	0
d-12	d-12	d-12 f	d-12 e	d-12 d	d-12 c	d-12 b	d-12 a
	"						

"H": VP

"L": NORMAL

FIG. 25



d-7: SHOW VC-AIS STATE ("H": AIS)

d-8: CANCELING TIMER FOR VC-AIS 2.5 SECOND COUNTER, COUNTED UP

EVERY 156msec

d-9 : SHOW VC-RDJ STATE ("H": RDJ)

d-10: CANCELING TIMER FOR VC-RDI,

2.5 SECOND COUNTER,

COUNTED UP EVERY 156msec

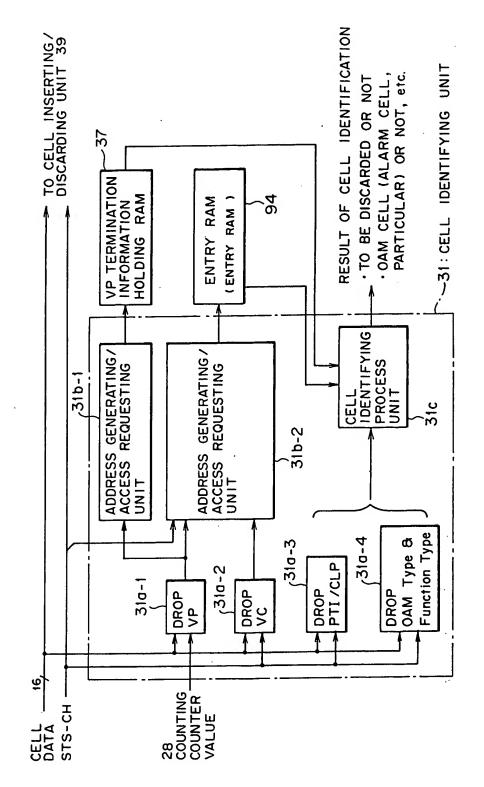


FIG. 27

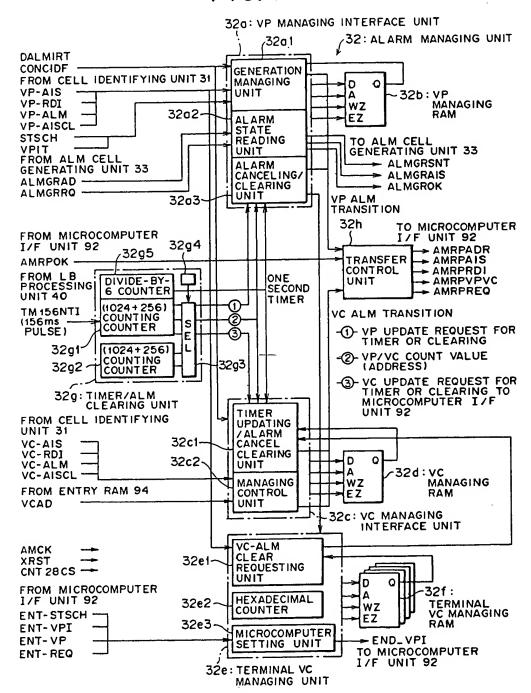
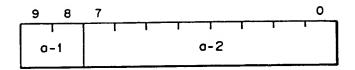


FIG.28



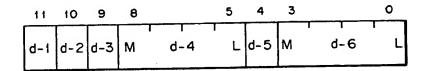
a-1: STS-3c IDENTIFICATION ADDRESS

00: STS-3c #1 / STS-12c

01:STS-3c #2 10:STS-3c #3 11:STS-3c #4

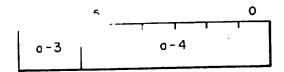
o-2: VPI (8 bits) OF ALM Cell WHEN VPI IS LESS THAN 8bits, ADD "O" TO HIGH ORDER bits

FIG.29



- d-1: SHOW VP-AIS STATE ("H": AIS)
- d-2: FLAG "500mf" SHOWING WHETHER ALARM CELL IS
   SENT WITHIN THE INITIAL 500msec AFTER GETTING
   INTO VP -AIS STATE OR SONET ALM STATE
   ("L":SEND COMPLETE)
   ("H":SEND NOT COMPLETE)
- d-3: FLAG "1sF" USED TO SEND ALARM CELL AT 1 sec INTERVALS
- d-4: VP-AIS CANCELING TIMER, 2.5 SECOND COUNTER, COUNTED UP EVERY 156 msec
- d-5 : SHOW VP-RDI STATE ("H":RDI)
- d-6: VP-RDI CANCELING TIMER, 2.5 SECOND COUNTER, COUNTED UP EVERY 156 msec

FIG. 30



a-3: STS-3c IDENTIFICATION ADDRESS

00: STS-3c#1 /STS-12c

O1: STS-3c#2 10: STS-3c#3 11: STS-3c#4

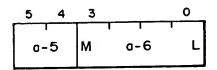
o-4: VC-AIS/RDI MANAGING INTERNAL ADDRESS (VC-ALM ADDRESS SET IN ENTRY RAM)

(0~63)

~32f  $\sim$ 32f#4. VP OF ch48~63 #1. VP OF ch48~63 #2. VP OF ch48~63 #3. VP OF ch48~63 #2. VP OF ch 16~31 #1, VP OF ch16~31 #3. VP OF ch 16~31 #4. VP OF ch 16~31 - RAM 2 --RAM 4 CLEAR REQUEST TO VC ALARM STATE MANAGING RAM #4. VP OF ch32~47 #2. VP OF ch32~47 #3. VP OF ch32~47 # 1. VP OF ch00~15 #2. VP OF ch00~15 #3. VP OF ch00~15 #4. VP OF ch00~15 #1. VP OF ch32~47 - RAM 1 --RAM3 -32f~ 32f~ 32e1b H 32e1: VC-ALM CLEAR REQUESTING UNIT COMPARING 32e1a 32e: TERMINAL VC ( MANAGING UNIT HEXADECIMAL COUNTER VP OF RECEIVED
AIS CELL # OF RECEIVED\_ VP-AIS CELL CLEAR COMPLETE 32e2

F16.3

FIG.32



a-5: STS-3c IDENTIFICATION ADDRESS

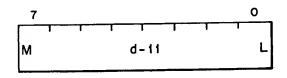
00: STS-3c #1/STS-12c

01: STS-3c #2 10: STS-3c #3 11: STS-3c #4

a-6 : LOW ORDER 4bits OF VC TERMINATION

SETTING ch (6bits)

FIG. 33



d-11: HOLD VPI OF VPI/VCI TO WHICH VC TERMINATION IS SET

FIG.34

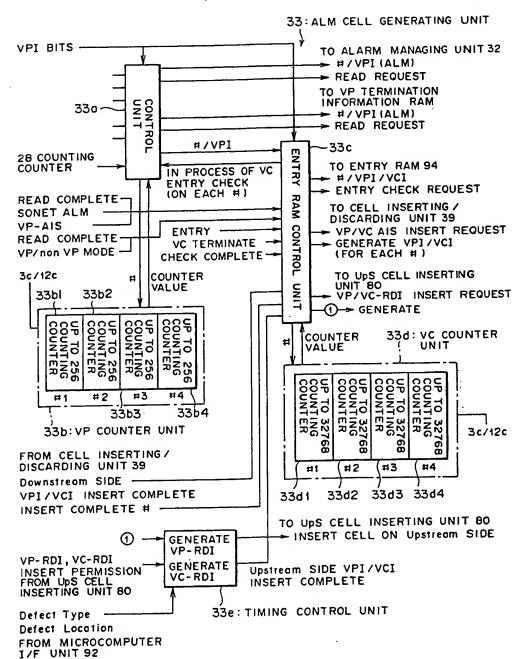


FIG. 35

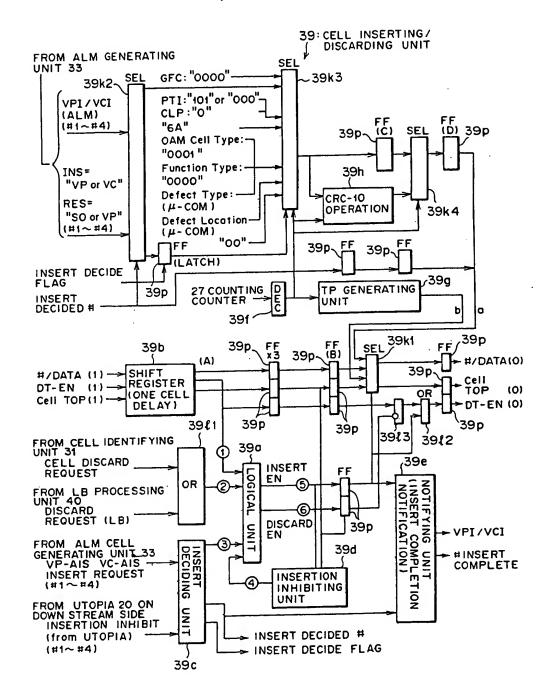


FIG.36

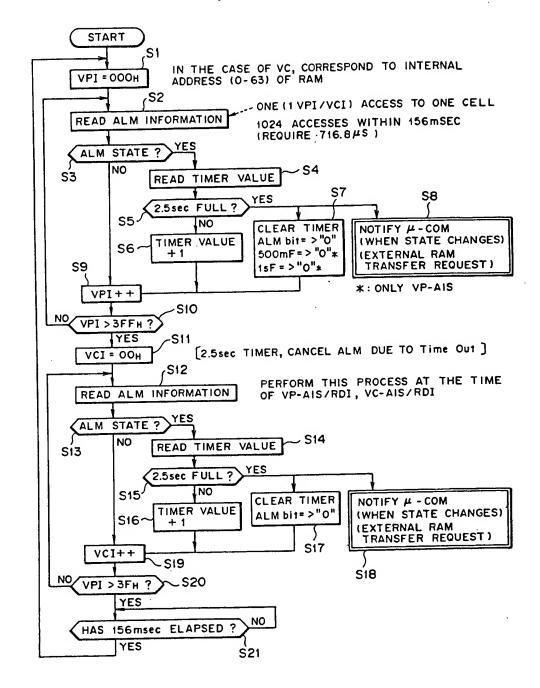


FIG. 37

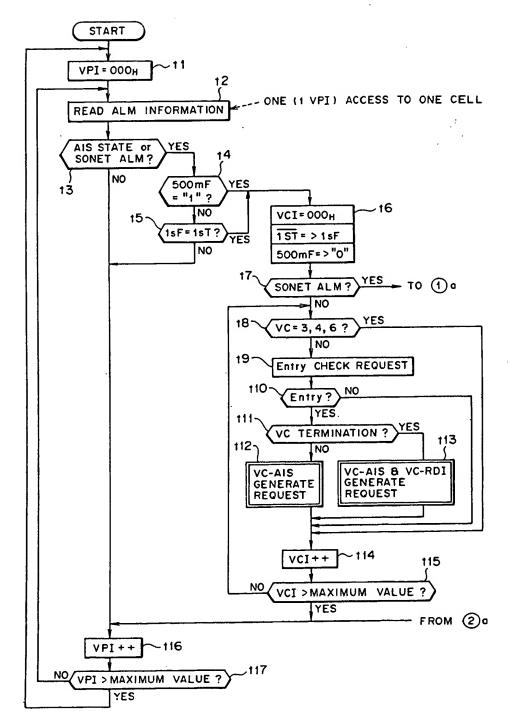
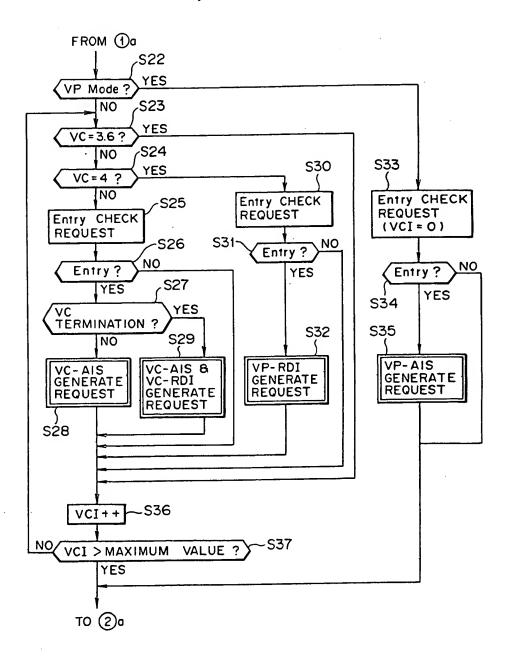
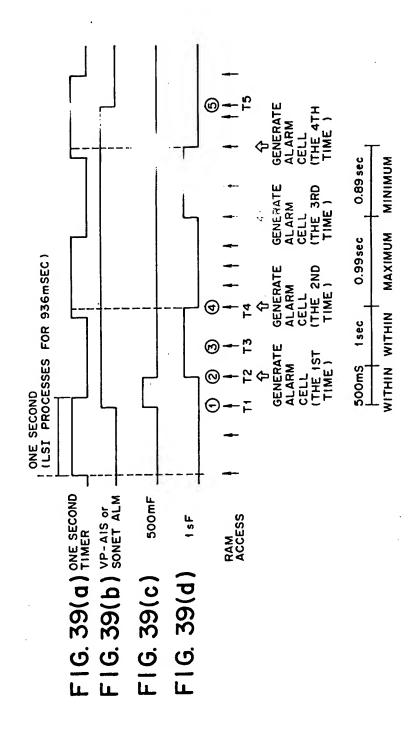


FIG. 38





MICROCOMPUTER
I/F UNIT 92 LBREOCH(1:0)
LBREOCH(1:0)
LBINSDT (15:0) TRANSFER EN INSERT CELLINFORMATION TO UPS CELL INSERTING UNIT 80 744: DP-RAM ~45:TIMER **▼ SIDEN** 40: LOOP BACK

PROCESSING UNIT 8/≷ LB2 GENERATING UNIT PROCESS LBGEN 44-2 MICROCOMPUTER I/F UNIT 92 VPIBIT 1 (2:0) VPIBIT 2 (2:0) VPIBIT 4 (2:0) VPIBIT 4 (2:0) LBTIMR SP-RAM Single Poot RAM 48: INITIALIZING UNIT TAGCTR(31:0)-FROM UTOPIA10 ON DOWNSTREAM SIDE CONCIRT CONCIDE LB11 LBSET1 DP-RAM CTR28(4:0) -FROM UPS CELL INSERTING UNITBO INSERT PERMISSION Port B TO PG UNIT 93 LBINSOK FROM PortA + LBINIT MICROCOMPUTER
1/F UNIT 92
TRANSFER
INFORMATION
SDDTEN 44-1 TO CELL PROCESSING UNIT 30, PM PROCESSING UNIT 50, Ups CELL INSERTING UNIT 80 TAGCTR(31:0)

TAGCTR(31:0)

CH128CTR(6:0) LBINT HLBCHKOK-XRST .47:COUNTER UNIT 42 œ 2 TIMACSEN -RECEIVE CONFIRMATION PROCESSING UNIT LBCHECK L N N N œ FROM MICROCOMPUTER 1/F UNIT 92 TRANSFER INFORMATION TRREO
LB-RW
TRADD(6:0)
TRDATA(15:0) - CHI 28CTR(6:0)→ FROM CELL PROCESSING UNIT 30 LBADR(4:0) -VPI VCI (15:0) -- CTR28(4:0) - DATA(15:0) - STSCH (1:0) - SIDNG - LBCHK - LBCHKON - LBCHKSCP LBRETRY L TIMACSEN 156ms & Tog CTR TAG 156M TO CELL PROCESSING
UNIT 30
LB RECEIVING
PROCESS RESULT
L BDWOK TO UDS CELL
INSERTING UNIT BO
INSERT CELL
INFORMATION TO MICROCOMPUTER I/F UNIT 92 RECEIVED EN -CTR28(4:0) STSCH(1:0) –
SIDNG
– BCHK
– LBCHKON
– LBCHKSCP HEFFOCL CTR28(4:0) CTR28(4:0) CTR28(4:0) CTR28(4:0) CTR28(4:0) CTR28(4:0) CTR28(4:0) CTR28(4:0) DATA(15:0) **→** LBFIFOCL PROCESS 4 FROM CELL PROCESSING UNIT SO CELL ENTRY INFORMATION VPMDCK ES (1:0) VPMDCK ES (1:0) VP-SEG-LB VC-SEG-LB FROM MICROCOMPUTER I/F UNIT 92 LIDMUX(15:0)— CELTPLB
DATADS(15:0)
DTENDS
STSCHDS(1:0) FROM UTOPIA 10 ON DOWNSTREAM AMCK → XLGRST → RECEIVED CELL DATA SIDE

FIG.41

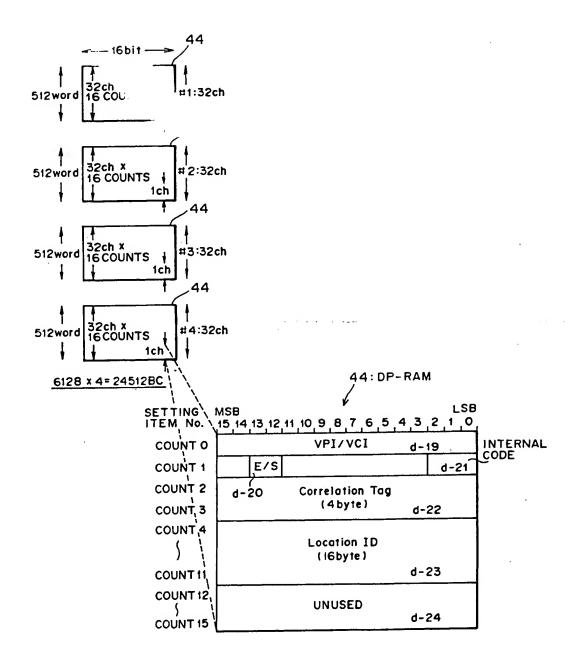


FIG.42

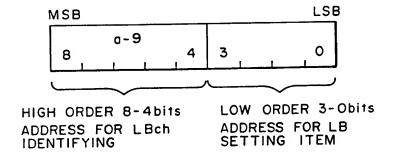
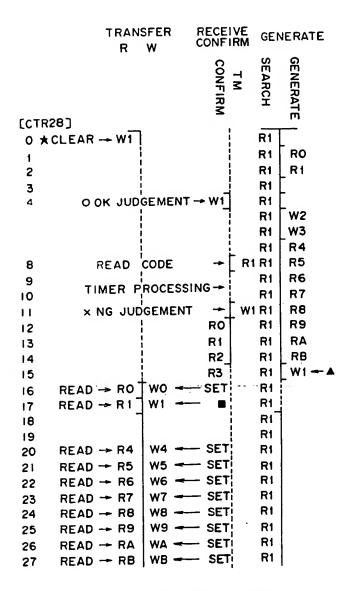


FIG. 43



- ★: CLEAR code AFTER OK/NG CODE IS READ
- O: WRITE OK code RESULTING FROM OK JUDGEMENT
- X: WRITE NG code RESULTING FROM TIME OUT
- ■: WRITE transmit wait code AT THE TIME OF MICROCOMPUTER SETTING AND CLEAR TIMER
- A: WRITE receive wait code WHEN LB CELL IS GENERATED

FIG. 44

 15 14 13 12 11 <sup>-</sup>	10 9 8 7 6 5	4 3 2 1 0
GFC	VPI	VCI
	VCI	PTI CL
	UNUSED (HEC)	
OAM CELL TYPE FUNC	TION TYPE LOOPBACK-I	NDICATION
	CORRELATION TAG	
	(4 byte)	
LOOF	BACK LOCATION ID (OP)	rional )
	(16 byte)	
	*****	
	SOURCE ID (OPTIONAL	}
	(16.byte)	
	•	
	UNUSED	
	(8 byte)	
RESERVED	EDC (CRC	:-10 )

FIG.45

FIG. 46

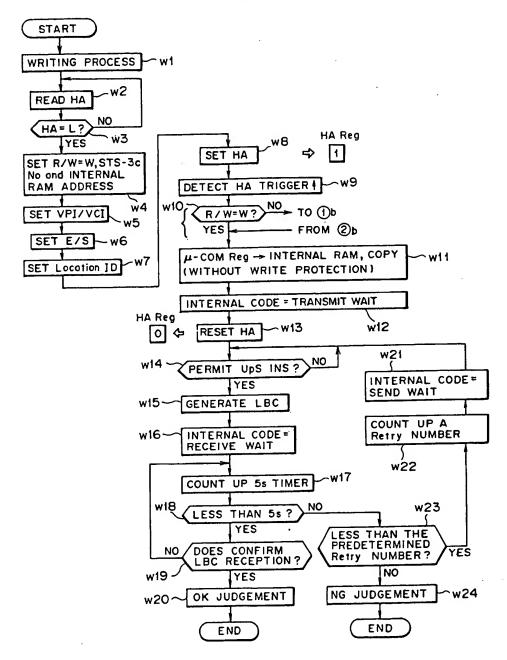


FIG.47

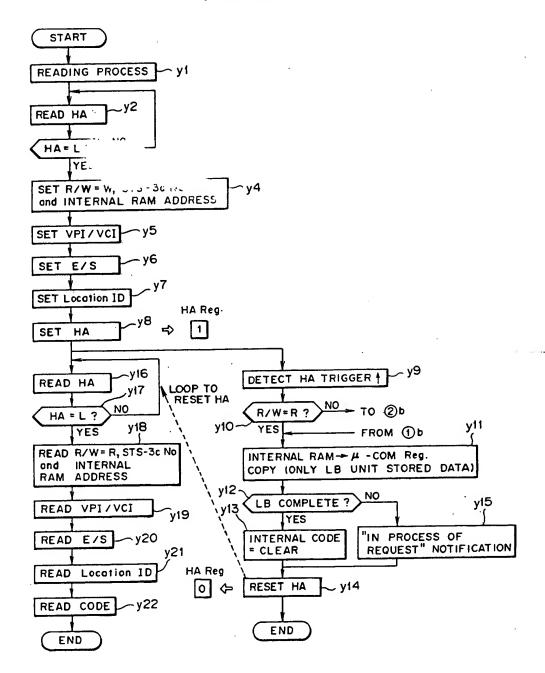


FIG. 48

